AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings of claims in the application:

1. (Currently Amended) An active pixel image sensor comprising:

a plurality of direct injection unit cells, each adapted to generate charge in response to photons incident thereon; ~~and~~

array elements adapted to sum charge from at least two unit cells at a focal plane of said image sensor, wherein said array elements comprise[[:]] a plurality of charge integration capacitors, each charge integration capacitor associated with an amplifier and configured to sum charges from at least two unit cells; and

a plurality of amplifier selector circuits, each amplifier selector circuit configured to steer charge from a plurality of said unit cells to a plurality of said amplifiers, in response to a plurality of control signals; wherein:

each of said amplifier selector circuits receives output from at least three of said unit cells; and

output from at least one of said at least three unit cells is also input to at least one other amplifier selector circuit.

2. (Previously Presented) An image sensor according to claim 1, wherein:

each of said unit cells comprises:

a unit cell charge integration capacitor capable of storing charge generated in response to said photons; and

a charge transfer transistor connected to said unit cell charge integration capacitor and adapted to transfer charge from said each unit cell when activated; and

said array elements further comprise:

a line decoder adapted to activate the charge transfer transistors of one or more lines of unit cells; and

a column selector adapted to activate one or more columns of unit cells and to combine the charge transferred by activated charge transfer transistors of said activated columns.

3. (Original) An image sensor according to claim 2 and wherein said array elements comprise adjacent line means adapted to indicate to said line decoder to activate at least two adjacent lines and to said column selector to select one column thereby to combine charge from the corresponding unit cells in adjacent lines.

4. (Original) An image sensor according to claim 2 and wherein said array elements comprise adjacent column means adapted to indicate to said line decoder to activate one line and to said column selector to combine charge of at least two columns thereby to combine charge from at least two unit cells in adjacent columns.

5. (Original) An image sensor according to claim 2 and wherein said array elements comprise block means adapted to indicate to said line decoder to activate U adjacent lines and to said column selector to combine charge of V columns thereby to combine charge from UxV unit cells in a UxV block.

6. (Original) An image sensor according to claim 3 and comprising interlace means adapted to produce video output from said image sensor.in an interlace mode.

7. (Original) An image sensor according to claim 6 and wherein said interlace means comprises means adapted to activate said adjacent line means to combine charge of pairs of unit cells in adjacent lines beginning with the odd lines adapted to an odd field output and of adjacent lines beginning with the even lines adapted to an even field output.

8. (Original) An image sensor according to claim 4 and comprising intercolumn means adapted to produce video output from said image sensor in an intercolumn mode.

9. (Original) An image sensor according to claim 8 and wherein said intercolumn means comprises means adapted to activate said adjacent column means to combine charge of pairs of adjacent columns beginning with the odd columns adapted to an odd field output and of adjacent columns beginning with the even columns adapted to an even field output.

10. (Original) An image sensor according to claim 5 and comprising block interlace means adapted to produce video output from said image sensor in a block interlace mode.

11. (Original) An image sensor according to claim 10 and wherein said block interlace means comprises means adapted to activate said block means to combine charge of 2x2 blocks wherein the blocks of an odd field output begin with the block whose upper left-hand unit cell is in the first column, first line and wherein the blocks of an even field output begin with the block whose upper left-hand unit cell is in the second column, second line.

12. (Currently Amended) An active pixel image sensor comprising:

a plurality of direct injection unit cells, each adapted to generate charge in response to photons incident thereon; ~~and~~

array elements adapted to change a resolution of the output of said image sensor at a focal plane of said image sensor by summing the charge generated by at least two unit cells of said plurality of unit cells, wherein said array elements comprise[[:]] a plurality of charge integration capacitors, each charge integration capacitor associated with an amplifier and configured to sum charges from at least two unit cells; and

a plurality of amplifier selector circuits, each amplifier selector circuit configured to steer charge from a plurality of said unit cells to a plurality of said amplifiers, in response to a plurality of control signals; wherein:

each of said amplifier selector circuits receives output from at least three of said unit cells; and

output from at least one of said at least three unit cells is also input to at least one other amplifier selector circuit.

13. (Previously Presented) An image sensor according to claim 12, wherein:

each of said unit cells comprises:

a unit cell charge integration capacitor capable of storing charge generated in response to said photons; and

a charge transfer transistor connected to said unit cell charge integration capacitor and adapted to transfer charge from said each unit cell when activated; and

said array elements further comprise:

a line decoder adapted to activate the charge transfer transistors of one or more lines of unit cells; and

a column selector adapted to activate one or more columns of unit cells and to combine the charge transferred by activated charge transfer transistors of said activated columns.

14. (Original) An image sensor according to claim 13 and wherein said array elements comprise adjacent line means adapted to indicate to said line decoder to activate at least two adjacent lines and to said column selector to select one column thereby to combine charge from the corresponding unit cells in adjacent lines.

15. (Original) An image sensor according to claim 13 and wherein said array elements comprise adjacent column means adapted to indicate to said line decoder to activate one line and to said column selector to combine charge of at least two columns thereby to combine charge from at least two unit cells in adjacent columns.

16. (Original) An image sensor according to claim 13 and wherein said array elements comprise block means adapted to indicate to said line decoder to activate U adjacent lines and to

said column selector to combine charge of V columns thereby to combine charge from UxV unit cells in a UxV block.

17. (Original) An image sensor according to claim 14 and comprising interlace means adapted to produce video output from said image sensor in an interlace mode.

18. (Original) An image sensor according to claim 17 and wherein said interlace means comprises means adapted to activate said adjacent line means to combine charge of pairs of unit cells in adjacent lines beginning with the odd lines adapted to an odd field output and of adjacent lines beginning with the even lines adapted to an even field output.

19. (Original) An image sensor according to claim 13 and comprising intercolumn means adapted to produce video output from said image sensor in an intercolumn mode.

20. (Original) An image sensor according to claim 19 and wherein said intercolumn means comprises means adapted to activate said adjacent column means to combine charge of pairs of adjacent columns beginning with the odd columns adapted to an odd field output and of adjacent columns beginning with the even columns adapted to an even field output.

21. (Original) An image sensor according to claim 13 and comprising block interlace means adapted to produce video output from said image sensor in a block interlace mode.

22. (Original) An image sensor according to claim 21 and wherein said block interlace means comprises means adapted to activate said block means to combine charge of 2x2 blocks wherein the blocks of an odd field output begin with the block whose upper left-hand unit cell is in the first column, first line and wherein the blocks of an even field output begin with the block whose upper left-hand unit cell is in the second column, second line.

23. (Currently Amended) A method comprising:

generating charge in response to photons incident on a plurality of ~~direct injection~~ unit cells of an active pixel image sensor;

supplying charge, via a first plurality of overlapping sets of column lines, each set comprising at least three column lines and each column line connected to unit cells belonging to a corresponding column, to a corresponding first plurality of amplifier selector circuits, each amplifier selector circuit configured to selectively steer charge supplied via a corresponding overlapping set of column lines to a plurality of amplifiers in response to a plurality of control signals; and

summing charge from at least two of said plurality of unit cells, at each of a plurality of charge integration capacitors, each of which is associated with an amplifier, at a focal plane of said image sensor.

24. (Original) A method according to claim 23 and wherein said summing comprises:

activating charge transfer transistors of one or more lines of unit cells;

activating one or more columns of unit cells; and

combining the charge transferred by activated charge transfer transistors of said activated columns.

25. (Original) A method according to claim 23 wherein said summing comprises activating at least two adjacent lines and selecting one column thereby to combine charge from the corresponding unit cells in adjacent lines.

26. (Original) A method according to claim 23 and wherein said summing comprises activating one line and combining charge of at least two columns thereby to combine charge from at least two unit cells in adjacent columns.

27. (Original) A method according to claim 23 and wherein said summing comprises activating U adjacent lines and combining charge of V columns thereby to combine charge from UxV unit cells in a UxV block.

28. (Original) A method according to claim 25 and comprising producing video output from said image sensor in an interlace mode.

29. (Currently Amended) A method according to claim 28 and wherein said producing comprises combining charge of pairs of unit cells in adjacent lines beginning with the odd lines for an odd field output and of adjacent lines beginning with the even lines for an even field output.

30. (Original) A method according to claim 26 and comprising producing video output from said image sensor in an intercolumn mode.

31. (Original) A method according to claim 30 and wherein said producing comprises combining charge of pairs of adjacent columns beginning with the odd columns for an odd field output and of adjacent columns beginning with the even columns for an even field output.

32. (Original) A method according to claim 31 and comprising producing video output from said image sensor in a block interlace mode.

33. (Original) A method according to claim 32 and wherein said producing comprises combining charge of 2x2 blocks wherein the blocks of an odd field output begin with the block whose upper left-hand unit cell is in the first column, first line and wherein the blocks of an even field output begin with the block whose upper left-hand unit cell is in the second column, second line.

34. (Currently Amended) A method comprising:

generating charge in response to photons incident on a plurality of unit cells of an active pixel image sensor;

supplying charge, via a first plurality of overlapping sets of column lines, each set comprising at least three column lines and each column line connected to unit cells belonging to a corresponding column, to a corresponding first plurality of amplifier selector

circuits, each amplifier selector circuit configured to selectively steer charge supplied via a corresponding overlapping set of column lines to a plurality of amplifiers in response to a plurality of control signals; and

changing a resolution of the output of said image sensor at a focal plane of said image sensor by summing the charge generated by at least two of said plurality of unit cells, at each of a plurality of charge integration capacitors, each of which is associated with an amplifier.

35. (Original) A method according to claim 34 and wherein said changing comprises:

activating charge transfer transistors of one or more lines of unit cells;

activating one or more columns of unit cells; and

combining the charge transferred by activated charge transfer transistors of said activated columns.

36. (Original) A method according to claim 34 wherein said changing comprises activating at least two adjacent lines and selecting one column thereby to combine charge from the corresponding unit cells in adjacent lines.

37. (Original) A method according to claim 34 and wherein said changing comprises activating one line and combining charge of at least two columns thereby to combine charge from at least two unit cells in adjacent columns.

38. (Original) A method according to claim 34 and wherein said changing comprises activating U adjacent lines and combining charge of V columns thereby to combine charge from UxV unit cells in a UxV block.

39. (Original) A method according to claim 36 and comprising producing video output from said image sensor in an interlace mode.

40. (Original) A method according to claim 39 and wherein said producing comprises combining charge of pairs of unit cells in adjacent lines beginning with the odd lines for an odd field output and of adjacent lines beginning with the even lines for an even field output.

41. (Original) A method according to claim 37 and comprising producing video output from said image sensor in an intercolumn mode.

42. (Original) A method according to claim 41 and wherein said producing comprises combining charge of pairs of adjacent columns beginning with the odd columns for an odd field output and of adjacent columns beginning with the even columns for an even field output.

43. (Original) A method according to claim 42 and comprising producing video output from said image sensor in a block interlace mode.

44. (Original) A method according to claim 43 and wherein said producing comprises combining charge of 2x2 blocks wherein the blocks of an odd field output begin with the block whose upper left-hand unit cell is in the first column, first line and wherein the blocks of an even field output begin with the block whose upper left-hand unit cell is in the second column, second line.

45. (Canceled)

46. (Canceled)